High Level Cascaded Multilevel Inverter with Low Values of THD Used for Electric Vehicles

Manu. C¹, Dr. K. Mekala²

¹ME Student, Mahendra College of Engineering, Salem, Tamilnadu, India. ²Assistant Professor, Mahendra College of Engineering, Salem, Tamilnadu, India.

Abstract—A multilevel inverter is a power electronic device, used in different applications. Changing many drawbacks and added to many advantages to make different levels inverter and also reduced the switches. This help to reduce the switching stress and lower total harmonic distortion (THD). This paper explained a high level of cascaded multilevel inverter with less number of switches and reduce the size. Here a Twenty five level converter will be simulated and its effect on the harmonic spectrum will be analyzed. This will be analyzed with the help of MATLAB/SIMULINK.

Keywords—Cascaded Multilevel Inverter, High Level, THD

I. INTRODUCTION

Now days an energy storage system plays an important role. Different types of batteries, such as lead-acid or lithium batteries are commonly used. A large number of battery cells need to be connected in series to boost the voltage level used in motor drive and other applications. Due to manufacturing defect, the internal characters of such batteries are different and therefore the terminal voltage and state-of-charge (SOC) will be also different.

An symmetrical or asymmetrical cascaded multi-level inverter help to increase the voltage level with reduced number of switching circuit and it produces a different level sinusoidal like waveform with less harmonics and also decreases the dv/dt stresses on the load. . Due to increasing energy demand more consumers depending on the renewable energy sources. The output of renewable energy sources is DC. To drive AC loads it convert from dc to ac. An inverter help this changes. By using the cascaded multilevel inverters required number of output voltage levels can be obtained by using different number of dc voltage sources.

In this project, a twenty five level cascaded multilevel converter which involves both battery energy management and motor drives. In the proposed technology, each battery cell can be connected to a half-bridge converter. The output all half bridges are staircase shape dc voltage. This staircase voltage

www.ijaers.com

converts to ac by using H-bridge converter. The outputs of the converter are multilevel voltages with less harmonics which is helpful to improve the performance of the motor drives.

II. EXISTING SYSTEM

2.1 Seven Level Multlevel Invereter

In seven level multilevel inverter used 10 Switches as shown in Figure 1 is built with 3 dc sources. The half bridge uses 6 switches and 3 voltage sources have same magnitude. Output of this connect to H-bridge. H bridge consist of 4 switches. By using control signals, operating these switches at proper interval time to obtain 7 levels with positive and negative half cycles. Table 1 represent the switching sequence of Seven level converter. Three voltage sources are V1,V2 and V3, each source connected in cascaded with other sources through a circuit consists of one switch and one diode. The output voltage of this circuit consist of only in positive polarity with a number of levels. This positive signal given to H-bridge circuit is to get both positive and negative polarity. Figure 1 shows 7 level multilevel inverter and table1 shows its switching sequence

First turning ON the switch S1, S4, S6,S7 and S10, and turn OFF S2, S3, S5, S8, and S9. The output voltage +1Vdc (first level) is produced across the load. Likewise turning ON the switches S1, S3, S6, S7 and S10 and turn OFF S2, S4,S5, S8 and S9 to produce voltage +2Vdc (second level) output across the load. Again the process will continue for the voltage level +3Vdc levels can be accomplished by turning ON S1, S3, S5, S7 and S10 switches and turn OFF switches S2,S4,S6,S8,and S9. In zero sequence switches S2,S4,S6,S9 and S10 turn ON and switches S1,S3,S5,S7 and S8 are turn OFF.



Fig.1. Seven Level Main Circuit

In -1Vdc level switches S1, S4, S6, S8 and S9 turned ON and switches S2, S3, S5, S7, and S10 are turned OFF. In -2Vdc switches S1, S3, S6, S8 and S9 are turned ON and switches S2, S4, S5, S7 and S10 are turned OFF. In -3Vdc switches S1, S3, S5, S8 and S9 are turned ON and switches S2,S4,S6,S7 and S10 are turned off.

Add these level to obtained the seven level output. The switching sequence for seven level inverter as shown in table1. Output wave form and THD values as shown in fig. 2 and 3.

Table - 1Switching Sequence for 7 Level Invereter

Voltage	S1	S	S	S	S	S	S	S	S	S
Level		2	3	4	5	6	7	8	9	10
0	0	1	0	1	0	1	0	0	1	1
Vdc	1	0	0	1	0	1	1	0	0	1
2Vdc	1	0	1	0	0	1	1	0	0	1
3Vdc	1	0	1	0	1	0	1	0	0	1
-Vdc	1	0	0	1	0	1	0	1	1	0
-2Vdc	1	0	1	0	0	1	0	1	1	0
-3Vdc	1	0	1	0	1	0	0	1	1	0



Fig. 2. Output wave form of Seven Level Inverter

THD values of Seven level converter is 22.73 %. This value can be reduced by increasing the level of converter



Fig. 3. THD values of Seven level conv

III. PROPOSED SYSTEM

3.1 Twenty Five Level Converter

25 Levels converter used 12 switches, four cells of equal or unequal voltage level in the ratio of 1:2:4:5. Connection diagram as shown in fig. 4. The three voltages are arranged in the ratio of 1:2:4:5 and to obtain the different votage levels such as 0 level, positive level (1Vdc to 12Vdc) and negative level (-1Vdc to -12 Vdc). The 4 voltage sources are controlled by 8 swithes S1, S2, S3, S4, S5, S6, S7 and S8. The output of this converter is positive pulse only, then it given to H bridge inverter to get fifteen level output by triggering the switches at required time intervel.

3.2 Pulse Generation Circuit

Sinewave voltage is pass through modulating circuit to obtain positive peak only, then it move to differnet logical operation circuit to obtain the different level of pulses. Add these signal to get 12 level positive step wave. Then it combine by proper arrangement with signal coming from relay circuit to get pulses A ,B, C and D as shown in fig. 5. This pulses given to multi port switch box with different sequence to obtained different gate pulses S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11 and S12 as shown in fig. 6.



Fig. 4. Twenty Five Level Main Circuit

From fig. 4, first turning ON the switch S1, S4, S6, S7 and S10, and turn OFF S2, S3, S5, S8, and S9. The output Voltage is +1Vdc. (first level) is produced across the load. In second level turning ON the switches S1, S3, S6, S7 and S10 and turn OFF S2, S4,S5, S8 and S9 to produce voltage +2Vdc output across the load. Again the process will continue for the voltage level +3Vdc levels can be accomplished by turning ON S1, S3, S5, S7 and S10 switches and turn OFF switches S2,S4,S6,S8,and S9. In fourth level switches S2, S4, S5, S7 and S10 are ON and switches S1, S3, S6, S8 and S9 are OFF. In fifth level switches S1, S4, S5, S7, S10 are ON and switches S2, S3, S6, S8, S9 are OFF. In sixth level S2, S3, S5, S7, S10 are ON and S1, S4, S6, S8 and S9 switches are turned OFF. In sevel (+7Vdc) level switches SS1, S3, S5, S7, S10 turned ON and S2, S4, S6, S8 and S9 are turned OFF. Similarly in 8.9, 10, 11, and 12 level can be obtained by control the switches based on the table 2. In zero sequence switches S2,S4,S6,S9 and S10 turn ON and switches S1,S3,S5,S7 and S8 are turn OFF.

[Vol-2, Issue-11,Nov-2015] ISSN: 2349-6495



Fig. 5. Twenty Five Level Control Circuit

In -1Vdc level switches S1, S4, S6, S8 and S9 turned ON and switches S2, S3, S5, S7, and S10 are turned OFF. In -2Vdc switches S1, S3, S6, S8 and S9 are turned ON and switches S2, S4, S5, S7 and S10 are turned OFF. In -3Vdc switches S1, S3, S5, S8 and S9 are turned ON and switches S2, S4, S6, S7 and S10 are turned off. In -4Vdc switches S2, S4, S5, S8 and S9 are ON and S1, S3, S6, S7, S10 are OFF. In -5Vdc, S1, S4, S5, S8 and S9 are ON and S2, S3, S6, S7, S10 are OFF position. In -6Vdc, S2, S3, S5, S8, S9 are ON and S1, S4, S6, S7, and S10 are OFF. IN -7Vdc level switches S1, S3, S5, S8, and S9 are turned ON and S2,S4, S6, S7, and S10 switches are OFF position. Similarly in -8, -9, -10, -11, and -12 level can be obtained by control the switches based on the table 2.

Add these level to obtained the twenty five level output. The switching sequence for twenty five level inverter as shown in table 2. Output wave form and THD values as shown in figure 7 and 8.



Fig. 6. Generation of Switching Signal by Using multi port switch box

Table - 2Switching Sequence for 25 Level Invereter

Voltage	S	S	S	S	S	S	S	S	S	S	S	S
Level	1	2	3	4	5	6	7	8	9	10	11	12
0	0	1	0	1	0	1	0	0	1	0	0	1
Vdc	1	0	0	1	0	1	Δ	1	1	Δ	•	1
			-	-	v	-	U	T	T	U	U	1
2Vdc	0	1	1	0	0	1	0	1	1	0	0	1

www.ijaers.com

Page | 4

4Vdc	0	1	0	1	1	0	0	1	1	0	0	1
5Vdc	0	1	0	1	0	1	1	0	1	0	0	1
6Vdc	1	0	0	1	0	1	1	0	1	0	0	1
7Vdc	0	1	1	0	0	1	1	0	1	0	0	1
8Vdc	1	0	1	0	0	1	1	0	1	0	0	1
9Vdc	0	1	0	1	1	0	1	0	1	0	0	1
10Vdc	1	0	0	1	1	0	1	0	1	0	0	1
11Vdc	0	1	1	0	1	0	1	0	1	0	0	1
12Vdc	1	0	1	0	1	0	1	0	1	0	0	1
-Vdc	1	0	0	1	0	1	0	1	0	1	1	0
-2Vdc	0	1	1	0	0	1	0	1	0	1	1	0
-3Vdc	1	0	1	0	0	1	0	1	0	1	1	0
-4Vdc	0	1	0	1	1	0	0	1	0	1	1	0
-5Vdc	0	1	0	1	0	1	1	0	0	1	1	0
-6Vdc	1	0	0	1	0	1	1	0	0	1	1	0
-7Vdc	0	1	1	0	0	1	1	0	0	1	1	0
-8Vdc	1	0	1	0	0	1	1	0	0	1	1	0
-9Vdc	0	1	0	1	1	0	1	0	0	1	1	0
-10Vdc	1	0	0	1	1	0	1	0	0	1	1	0
-11Vdc	0	1	1	0	1	0	1	0	0	1	1	0
-12Vdc	1	0	1	0	1	0	1	0	0	1	1	0



Fig. 7. THD values of Twenty Five level converter



Fig. 8 (a). Output wave form of Twenty Five Level Inverter



Fig. 8 (b). Output wave form of Twenty Five Level Inverter.

IV. RESULT

The waveforms and FFT analysis 25 levels MLI are shown in figure.7, 8. Compare this with seven levels MLI, the harmonics order reduced from 22.61 % to 3.81 %. Therefor increasing the level by using less number of switches to obtain high quality sinusoidal wave.

V. CONCLUSION

In this paper, Twenty Five level asymmetric cascaded multilevel inverter is submitteed. The Twent Five Level gives high quality output voltage close to sinusoidal Waves. It is improved performance than the 7 level Multilevel inverter, and also minimize the switching losses. The waveforms and FFT analysis 25 levels MLI are shown in figure.7, 8. Compare this with seven levels MLI, the harmonics order reduced from 22.61 % to 3.81 %. Therefor increasing the level by using less number of switches to obtain high quality sinusoidal wave.

REFERENCES

- M.Yilmaz and P. T.Krein, "Reviewof battery charger topologies, charging power levels, and infrastructure for plug-in electric and hybrid vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2151–2169, May 2013.
- [2] S. J. Huang, B. G. Huang, and F. S. Pai, "Fast charge strategy based on the characterization and evaluation of LiFePO batteries," *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1555–1562, Apr. 2013.
- [3] K. Chol-Ho, K. Moon-Young, and M. Gun-Woo, "A modularized charge equalizer using a batterymonitoring IC for series-connected Li-Ion battery strings in electric vehicles," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3779–3787, Aug. 2013.
- [4] K. Ilves, A. Antonopoulos, S. Norrga, and H. Nee, "A new modulation method for the modular multilevel converter allowing fundamental switching frequency," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3482–3494, Aug. 2012.
- [5] P. Sang-Hyun, P. Ki-Bum, K. Hyoung-Suk, M. Gun-Woo, and Y. Myung-Joong, "Single-magnetic cell-tocell charge equalization converter with reduced number of transformer windings," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2900–2911, Jun. 2012.
- [6] K. Chol-Ho, K. Moon-Young, P. Hong-Sun, and M. Gun-Woo, "A modularized two-stage charge equalizer with cell selection switches for seriesconnected lithiumion battery string in an HEV," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3764–3774, Aug. 2012.
- [7] Y. Ye, K. W. E. Cheng, and Y. P. B. Yeung, "Zerocurrent switching switched-capacitor zero-voltage-gap automatic equalization system for series battery string," *IEEE Trans. Power Electron.*, vol. 27, no. 7, pp. 3234– 3242, Jul. 2012.
- [8] L. Maharjan, T. Yamagishi, and H. Akagi, "Activepower control of individual converter cells for a battery energy storage system based on a multilevel cascade PWM converter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1099–1107, Mar. 2012.
- [9] B. P. McGrath and D. G. Holmes, "Enhanced voltage balancing of a flying capacitor multilevel converter using phase disposition (PD) modulation, "*IEEE Trans. Power Electron.*, vol. 26, no. 7, pp. 1933–1942, Jun. 2011.
- [10] A. Shukla, A. Ghosh, and A. Joshi, "Natural balancing of flying capacitor voltages in multicell inverter under PD

www.ijaers.com

carrier-based PWM," *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1682–1693, Jun. 2011.

- [11] S.Yarlagadda, T. T.Hartley, and I.Husain, "Abatterymanagement system using an active charge equalization technique based on a DC/DC converter topology," in *Proc. Energy Convers. Congr. Expo.*, 2011, pp. 1188– 1195.
- [12] K. Chol-Ho, K. Young-Do, and M. Gun-Woo, "Individual cell voltage equalizer using selective two current paths for series connected Li-ion battery strings," in *Proc. Energy Convers. Congr. Expo.*, 2009, pp. 1812–1817.
- [13] Y. C. Hsieh, C. S. Moo, and W. Y. Ou-Yang, "A bidirectional charge equalization circuit for seriesconnected batteries," in *Proc. IEEE Power Electron. Drives Syst.*, 2005, pp. 1578–1583.
- [14] N. H. Kutkut and D. M. Divan, "Dynamic equalization techniques for series battery stacks," in *Proc. 18th Int. Telecommun. Energy Conf.*, 1996, pp. 514–521.